Design of High Performance Three-input XOR/XNOR Circuit

Chien-Cheng Yu

Abstract

In this paper, we propose a 3-input XOR/XNOR circuit for low-voltage low-power applications. Several existing 3-input XOR/XNOR circuits and this proposed circuit have been fully simulated using HSPICE with a 0.35 μm CMOS technology from 3.3 V down to 2V supply voltage. The simulation results show that the proposed circuit has the benefits of better driving capability and lower power consumption as well as the least power-delay product than those of the existing circuits. Additionally, this circuit has a full voltage-swing in all internal nodes under 2V supply voltage or less. Thus, the proposed circuit is suitable for low-voltage, low-power applications.

Key Words : Low voltage, Full swing, XOR/XNOR circuit

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1. Introduction

In CMOS circuits, the power consumption is proportional to switching activity, capacitive loading, and the square of the supply voltage [1]-[2]. With the V_{DD}^2 relationship to power consumption, hence, lowering supply voltage is obviously the most direct and effective way of reducing the power consumption. However, as supply voltage is lowered, there exists various problems associated with lowering voltage, such as the driving capability decreasing and the noise margin reduction. Therefore, high performance and correct functionality of circuits must be guaranteed at low voltage as well.

The exclusive-OR (XOR) and exclusive-NOR (XNOR) gates are fundamental units in various digital logic systems, such as full adder, comparator, parity generator, and so forth. It is well known that a binary operator can be extended to accommodate multiple variables if the operation is both commutative and associative. Since the binary XOR and XNOR operation are both commutative and associative, both operators can be extended to multiple inputs. According to the properties of odd (XOR) and even (XNOR) functions, it can be shown that the function of 3-input XOR and 3-input XNOR are equivalent. Consequently, a straightforward method of implementing 3-input XOR function is to cascade two 2-input XOR (or XNOR). In this paper, we firstly propose a 2-input XNOR circuit that can operate correctly in all internal nodes. And then, based on the proposed 2-input XNOR configuration, two 2-input XNOR are constructed appropriately for the 3-input XOR/XNOR function.

As a general rule, the dynamic circuit implementations have higher switching activities than static implementation due to the need of precharging [2]. Hence, the XOR/XNOR circuits in this work were implemented using static design. Furthermore, due to the power-delay product is the merit of measurement, the

performances of all XOR/XNOR circuits are compared in terms of power-delay product. In summary, the proposed circuits are designed with the following objectives:

1) Fully static design

2) Low voltage operation (2V)

3) Minimizing power-delay product

2. The Existing 3-input XOR/XNOR Circuits

In this section, we will look closely at five of the most popular 3-input XOR/XNOR circuits to examine their suitability for low-voltage, low-power applications.

A. Complementary CMOS Logic

In complementary CMOS logic, as shown in Fig. 1, the pull-down and pull-up networks perform the Boolean function in a complementary way. This style has the benefits of high noise margins and no static power consumption. However, the longer delay time and higher power consumption result from the high input capacitance are unfavorable factors in using this kind style [2].

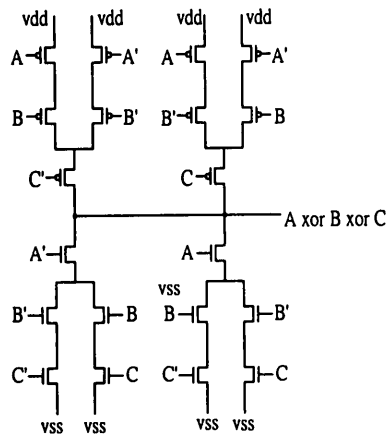

Fig.1 The complementary CMOS logic.

B. CMOS with Transmission Gate (TG)

Fig. 2 shows the CMOS with transmission gate (TG-CMOS) XOR circuit [3]-[4]. It is well known that combining an NMOS and a PMOS to carry on a transmission gate can pass both signals "0" and "1" with excellent performance. Additionally, the source node of the pass-transistor networks is connected to some input signals instead of the power lines. This advantage leads to the implementation of transmission gates in logic circuit design may even require a smaller number of transistors. Also, pass-transistor logics gain their speed advantage over CMOS due to their high logic functionality.

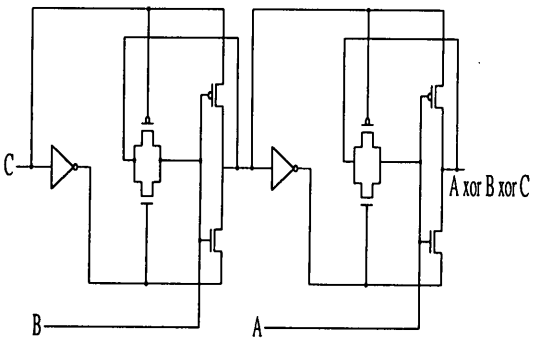

Fig.2 The TG-CMOS logic.

C. *Complementary pass-transistor logic(CPL)* [5]

The input capacitance in CPL is about half that of the CMOS configuration, which results in higher speed and lower power consumption. In addition, this style posses some interesting properties, such as good output driving capability, and fast differential stage.

However, in reduced supply voltage designs, it is crucial to take into account the problems of noise margins and speed degradation [5]. In other words, CPL can not perform well at lower supply voltage.

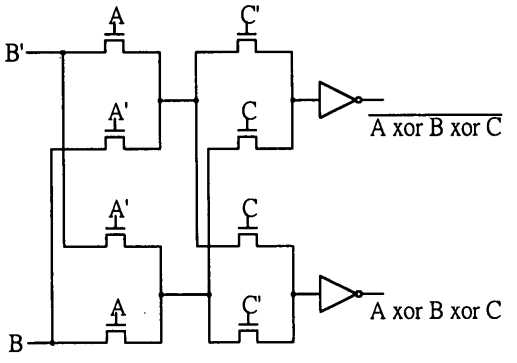

Fig.3 The CPL circuit.

D. Fang's XOR Circuit

From the application point of view, Fang [6] presented two 3-input XOR circuits with driving-enhanced capacity as shown in Figs. 4 and 5. Both circuits can operate well at supply voltage of 3.3V. However, as the supply voltage decreases to 2V, both of them have worse performance result from the cascaded design using non-complementary input signals.

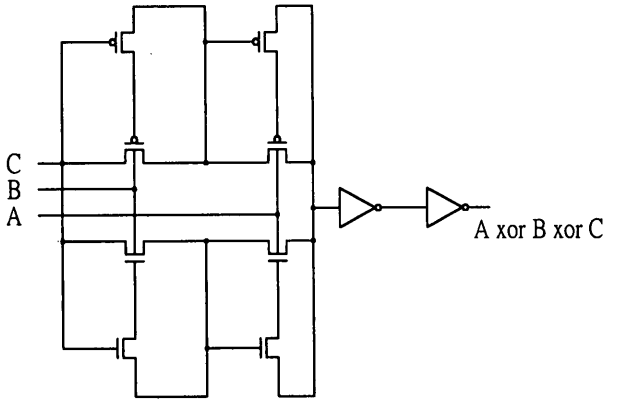

Fig.4 The Fang's direct design of XOR circuit.

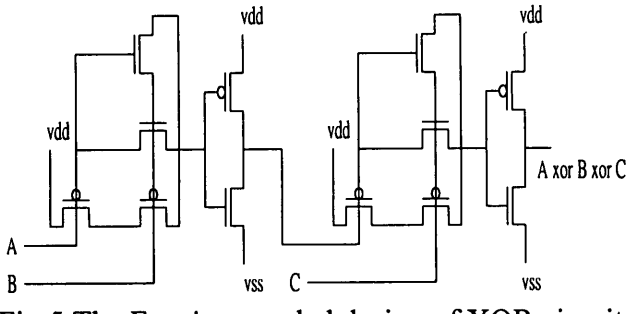

Fig.5 The Fang's cascaded design of XOR circuit.

3. The Proposed XOR/XNOR circuits

A. 2-input XNOR Circuit

The schematic for the proposed 2-input XNOR circuit is shown in Fig. 6(a). To analyze this structure, we use the complete set of input signals AB = 00,01,10,11. Firstly, consider the case when A = B = 0, the pull-up transistor MP2 is ON whereas all other transistors are OFF. Thus, the output node X then goes to good "1" through the pull-up transistor MP2. Next, consider the case when A=1, B=0, the pull-down transistor MN2 is OFF and all other transistors are ON. Meanwhile, both pull-up transistors MP1 and MP2 are activated. A similar argument leads to the third case when A=0, B=1. Finally, if A=B=1, then MP1, MN1 and MN2 are ON whereas MP2 is OFF. Hence, the voltage across MP1 is "1" and the output node X is "1".

These four states conform the XNOR operation and are summarized in Table I.

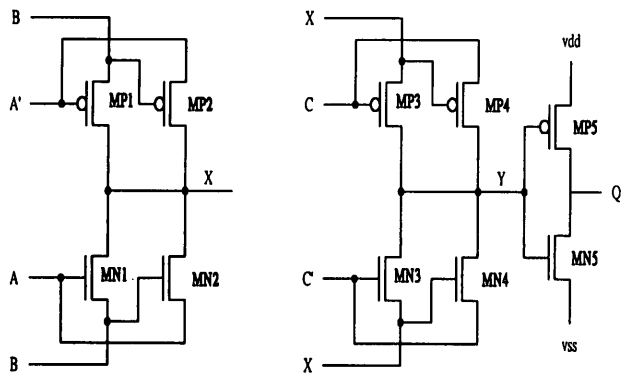

Fig.6 The proposed circuits: (a) 2-input XNOR; (b) 3-input XOR

B. 3-input XOR/XNOR Circuit

Based on the proposed 2-input XNOR configuration, two 2-input XNOR can be constructed appropriately for the XOR/XNOR function as illustrated in Fig.6(b).

It can be shown that a "0" output will occur at node Y when the input signals have an odd number of 1's to turn on either NMOS transistor MN3 or MN4, thereby providing a low resistance path from the output node to ground. For other input conditions, either PMOS transistor MP3 or MP4 will be ON when input signals have an even number of 1's. This produces a "1" output at node Y. We can easily verify that the output is Q = A⊕ B⊕C. For instance, if ABC=011, then MN2 and MP4 are "ON" and MP1, MP2, MN1, MP3, MN3, MN4 are "OFF", therefore, the output Q = 0. One more example, if ABC=010, then MN2, MP3, MP4, MN3 are "ON" and MP1, MP2, MN1, MN4 are "OFF", therefore, the output Q = 1.

These active states of the proposed 3-input XOR/XNOR circuit structure in all cases are summarized in Table II.

4. Simulation Results and Comparisons

The performance of our circuit was compared to several existing 3-input XOR/XNOR circuits. The characteristic of the Gray code is that only one bit in the code group changes when going from one number to the next. We use such arrangement to compare the performance of several existing 3-input XOR/XNOR circuits. All are implemented in 0.35μm CMOS technology from 3.3V down to 2V supply voltage.

Since internal nodes of TG-CMOS, CPL, and Fang's direct design style circuits do not have a full voltage swing, these circuits can not operate reliably at a 2V supply voltage. Therefore, they were excluded from the comparison.

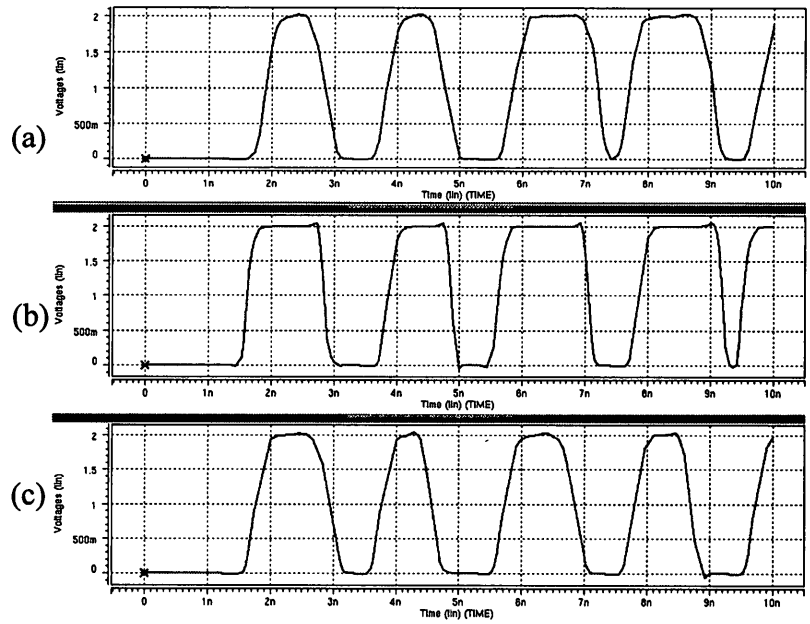

Fig.7 Simulation results for one complete set of transitions: (a)complementary CMOS logic; (b)Fang's cascaded design style circuit ; (c)proposed circuit

Our simulation results show that the proposed circuit provides a full voltage swing and operates well in all internal nodes under 2V supply voltage, as shown in Fig. 7. Additionally, as shown in Tables III and IV, the proposed circuit has some favorable properties:

1. The driving capability of the proposed circuit is better than that of complementary CMOS logic and Fang's cascaded design style circuits.
2. The power-delay product is 14% and 10% less than that of complementary CMOS logic and Fang's cascaded design style circuit, respectively.

5. Conclusion

In this paper, a new 3-input XOR/XNOR circuit configuration for static CMOS implementation has been proposed. According to the simulation results, it is evident that the proposed circuit has the advantages of good signal output levels

and the lowest power-delay product at low supply voltage. Additionally, the proposed circuit has the benefits of smaller time delay than that of the previous existing circuits. Thus, the proposed circuit is suitable for low-voltage, low-power applications.

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Table I The active state of the proposed 2-input XNOR circuit structure in all cases

A	B	MP1	MP2	MN1	MN2	X
0	0	OFF	**ON**	OFF	OFF	1
0	1	OFF	OFF	OFF	**ON**	0
1	0	ON	ON	**ON**	OFF	0
1	**1**	**ON**	OFF	ON	ON	1

Table II The active state of the proposed 3-input XOR/XNOR circuit structure in all cases

C	X	MP3	MP4	MN3	MN4	Y	Q
0	0	ON	**ON**	ON	OFF	0	1
0	1	ON	OFF	ON	**ON**	1	0
1	0	OFF	ON	**OFF**	OFF	1	0
1	**1**	**OFF**	OFF	OFF	ON	0	1

Table III Delay-time analysis of the existing and the proposed XOR circuits (in nano second)

State	000→001	001→011	011→010	010→110	110→111	111→101	101→100	100→000	**Average**
Fig.1	0.8491	0.8009	0.6847	0.7066	0.7924	1.0499	0.5444	0.8828	**0.7889**
Fig.2	Not work	Not work	Not work	Not work	Not work	Not work	Not work	Not work	Not work
Fig.3	Not work	Not work	Not work	Not work	Not work	Not work	Not work	Not work	Not work
Fig.4	Not work	Not work	Not work	Not work	Not work	Not work	Not work	Not work	Not work
Fig.5	0.5621	0.7906	0.7152	0.8104	0.5649	0.9028	0.7059	1.035	**0.7609**
Proposed	0.712	0.8903	0.6169	0.5129	0.6798	0.6963	0.6519	0.5401	**0.6625**

Table IV Power-delay product analysis of the existing and the proposed XOR circuits

Circuit	Average Delay Time (ns)	Power (μW)	Power-delay product (normalized)
Fig. 1	0.7889	260.28	1.138
Fig. 2	Not work	Not work	Not work
Fig. 3	Not work	Not work	Not work
Fig. 4	Not work	Not work	Not work
Fig. 5	0.7609	260.79	1.099
Proposed	0.6625	272.44	1

高性能三輸入互斥或/反互斥或電路之設計

余 建 政

摘 要

由於 CMOS 電路的功率散逸是和電壓平方(V_{DD}^2)成正比，因此，減少功率散逸最直接有效的方式是降低電壓。本文中，我們提出一個能工作在低電壓下的互斥或(XOR)電路。經由實驗可得，此電路可以工作在 2 伏特電壓。

關鍵字：低電壓，全擺幅，XOR/XNOR 電路

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